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**MIT ART, DESIGN AND TECHNOLOGY UNIVERSITY, PUNE**

**Department of Electronics and Communication Engineering**

**MIT SCHOOL OF ENGINEERING, PUNE**

**STRUCTURE AND SYLLABUS**

**FOR**

**M. Tech. ECE - Microelectronics & VLSI Design**

**UNDER FACULTY OF TECHNOLOGY**

**(w.e.f. 2018-2019)**

**UNDER FACULTY OF TECHNOLOGY**

**M. Tech. Mechanical Engineering (Mechatronics)**

**2017-Course**

**kundlik mali**

**M.Tech. (ECE - Microelectronics & VLSI Design) (MV)**

**(Minimum credits to be earned: 74)**

**SEMESTER-I**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Code** | **Course Name** | **Hours/week** | | | | **Maximum Marks** | | |
|  | **Lecture** | **Tutorial** | **Practical** | **Credits** | **CA** | **FE** | **Total** |
| 18MTMT105 | Advanced Mathematics | 3 | 1 | 0 | 4 | 40 | 60 | 100 |
| 20MTMV101 | Research Methodology | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 18MTMV103 | Digital Design Techniques | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 18MTMV104 | Analog CMOS Design | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 18MTMV1[31-33]  20MTMV134 | Elective - I | 3 | 0 | 0 | 3 | 40 | 60 | 100 |
| 18MTMV111 | Laboratory - I | 0 | 0 | 4 | 2 | 40 | 60\*\* | 100 |
| 18MTMV121 | Technical Seminar - I | 0 | 0 | 4 | 2 | 100 | -- | 100 |
| **Total** | | **15** | **1** | **8** | **20** | **340** | **360** | **700** |

**SEMESTER-II**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Code** | **Course Name** | **Hours/week** | | | | | **Maximum Marks** | | | |
|  | | **Lecture** | **Tutorial** | **Practical** | **Credits** | | **CA** | **FE** | **Total** | |
| 18MTMV201 | Low Power VLSI Design | | 3 | 1 | 0 | 4 | | 40 | 60 | 100 | |
| 18MTMV202 | Digital VLSI Circuits | | 3 | 0 | 0 | 3 | | 40 | 60 | 100 | |
| 18MTMV203 | Testing and Testability | | 3 | 0 | 0 | 3 | | 40 | 60 | 100 | |
| 18MTMV204 | VLSI CAD | | 3 | 0 | 0 | 3 | | 40 | 60 | 100 | |
| 18MTMV2[31-32] | Elective - II | | 3 | 0 | 0 | 3 | | 40 | 60 | 100 | |
| 18MTMV211 | Laboratory - II | | 0 | 0 | 4 | 2 | | 40 | 60\*\* | 100 | |
| 18MTMV221 | Mini Project | | 0 | 0 | 4 | 2 | | 100 | -- | 100 | |
| **Total** | | | **15** | **1** | **8** | **20** | | **340** | **360** | **700** | |

**CA = Continuous Assessment, FE= Final Examination,**

**\*\*Final Lab exam will be conducted with viva-voce of the respective practical (50 exam +10 viva = 60)**

**Coding for course/ subject: 17AE101,** Where; **17** = Year of BOS, **AE** = Branch Code, **1**= Semester No.,

**01 to N** = Sequence No of Subject. **For,** SE to BE & also PG follow the above scheme of regulation.

**SECOND YEAR ENGINEERING SCHEME**

**SEMESTER-III**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Code** | **Course Name** | **Hours/week** | | | | **Maximum Marks** | | |
| **Lecture** | **Tutorial** | **Practical** | **Credits** | **CA** | **FE** | **Total** |
| 18MTMV301 | High Speed Digital Design | 3 | 1 | 0 | 4 | 40 | 60 | 100 |
| 18MTMV302 | Mixed Signal VLSI Design | 3 | 1 | 0 | 4 | 40 | 60 | 100 |
| 18MTMV3[31-32] | Elective - III | 3 | 1 | 0 | 4 | 40 | 60 | 100 |
| 18MTMV3[33-34] | Elective - IV | 3 | 1 | 0 | 4 | 40 | 60 | 100 |
| 18MTMV321 | Technical Seminar - II | 0 | 0 | 4 | 2 | 40 | 60\*\* | 100 |
| 18MTMV322 | Project Phase - I | 0 | 0 | 4 | 2 | 40 | 60\*\* | 100 |
| **Total** | | **12** | **4** | **8** | **20** | **240** |  | **600** |

**SEMESTER-IV**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Course Code** | **Course Name** | **Hours/week** | | | | | **Maximum Marks** | | | |
|  | | **Lecture** | **Tutorial** | **Practical** | **Credits** | | **CA** | **FE** | **Total** | |
| 18MTMV421 | Project Phase - II | | 0 | 0 | 28 | 14 | | 100 | 200 | 300 | |
| **Total** | | | **0** | **0** | **28** | **14** | | **100** | **200** | **300** | |

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**\*\*Final Lab exam will be conducted with viva-voce of the respective practical (50 exam +10 viva = 60)**

**Coding for course/ subject: 17AE101,** Where; **17** = Year of BOS, **AE** = Branch Code, **1**= Semester No.,

**01 to N** = Sequence No of Subject. **For,** SE to BE & also PG follow the above scheme of regulation.

**LIST OF ELECTIVES**

|  |  |  |
| --- | --- | --- |
| **Elective** | **Course Name** | |
|
| Elective-I | 18MTMV131 | Neural Networks in VLSI |
| 18MTMV132 | VLSI Technology |
| 18MTMV133 | MEMS |
| 20MTMV134 | Solid State Devices |
| Elective-II | 18MTMV231 | Semiconductor Memory Design and Testing |
| 18MTMV232 | RF Circuit Design |
| Elective-III | 18MTMV331 | Biomedical Signal Processing |
| 18MTMV332 | Digital Design And Verification With HDI |
| Elective-IV | 18MTMV333 | ASIC Design |
| 18MTMV334 | System on Chip Design |